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| EWULogo.png | | **EAST WEST UNIVERSITY** | | |
| **Department of Computer Science and Engineering** | | |
| **B.Sc. in Computer Science and Engineering Program** | | |
| **Final Examination, Fall 2021** | | |
| **Course:** | | **CSE360 – Computer Architecture, Section 3** | | |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department** | | |
| **Full Marks:** | | **25** | | |
| **Exam Time:** | | **1 Hour 20 Minutes** | **Submission Time: 10 Minutes** | |
| **Note:** There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin. | | | | |
| 1. | Convert the infix expression (A+B) \* ((C-D) / E+F)/G -H to the postfix notation using Dijkstra’s algorithm. Show the sequence of steps in the stack. | | | [ CO2, C3, Mark: 4] |
| 2. | Compute the following expression using stack.  (A/B\*C) + (D-E) \* F+G | | | [ CO2, C3, Mark: 3] |
| 3. | Analyze and Compare zero-, one-, two-, and three- address machines by writing programs to compute the following expression for each of the four machines.  The instructions available for use are as follows:   |  |  |  |  | | --- | --- | --- | --- | | 0 Address | 1 Address | 2 Address | 3 Address | | PUSH M  POP M  ADD  SUB  MUL  DIV | LOAD M  STORE M  ADD M  SUB M  MUL M  DIV M | MOV (X←Y)  ADD(X←X+Y)  SUB (X←X-Y)  MUL (X←X \*Y)  DIV(X←X/Y) | MOVE (X←Y)  ADD(X←Y+Z)  SUB(X←Y-Z)  MUL(X←Y\*Z)  DIV(X←Y/Z) | | | | [ CO3, C5, Mark: 5] |
| 4. | A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 20 clock cycles. Thereafter, it takes 25 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 5 GHz.   1. Determine the length of the instruction cycle for the case of a string of 32S bytes. 2. What is the worst-case delay for acknowledging an interrupt if the instruction is non interruptible? 3. Repeat part (b) assuming the instruction can be interrupted at the beginning of each byte transfer. | | | [CO3, C3 Mark: 2+2+2] |
| 5. | Assume a pipeline with six-stages: fetch instruction (FI), decode instruction (DI), calculate addresses (CA), fetch operand (FO), execute instruction (EI), and write operand (WO). Draw a diagram for a sequence of 10 instructions, in which the second instruction is a branch that effects on instruction pipeline operation in which there are no data dependencies. | | | [CO4, C4, Mark: 3 |
| 6. | Consider a 16-bit processor in which the following appears in main memory, starting at location 393:   |  |  |  | | --- | --- | --- | | 393 | Load to AC | Mode | | 394 | 9XY | | | 395 | Next instruction | |   The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R3, which has a value of 521. There is also a base register that contains the value 258. The value of 9XY in location 394 may be part of the address calculation. Assume that location 535 contains the value 809, location 536 contains the value 810, and so on. Determine the effective address and the operand to be loaded for the following address modes.   1. Immediate 2. Direct 3. Indirect 4. PC relative 5. Displacement 6. Register 7. Register indirect. 8. Autoindexing with increment, using R3 | | | [ CO4, C4, Mark: 4] |

[NB: XY is the last two digits of your ID, e.g., if your ID is 2019-3-60-041, then the value of X is 3 and Y is 7]